

AMENDMENTS TO THE SPECIFICATION

Please amend the Abstract as follows:

A test circuit is included in an IC wafer for testing the reliability of ICs under high current stress. The test circuit includes two sensing transistors, a select transistor, and a resistor. The two ends of the resistor are coupled to two sense terminals through the two sensing transistors. One end of the resistor is also coupled to a first stress input terminal; the other end of the resistor is coupled to a second stress input terminal through the select transistor. When the test circuit is selected, the sensing and select transistors are turned on. A current path is formed between the two stress input terminals, and a voltage differential can be measured across the resistor using the two sense terminals. Row and column select circuits enable the rapid testing of many resistor sizes and configurations in an array of such test circuits. A method of testing reliability in an integrated circuit including an array of test circuits, each test circuit including a resistor. The method includes selecting a first test circuit from the array, measuring a pre-stress resistance value for the resistor in the selected test circuit, applying a high stress current across the resistor, removing the high stress current, and measuring a post-stress resistance value for the resistor. Other embodiments include measuring additional resistance values before applying and after removing the high stress current. One embodiment includes applying a positive voltage to one stress input terminal, and then testing a short sensing terminal for the positive voltage, both before and after applying the high stress current. These steps test for whether or not the high stress current has created a short in the test circuit.